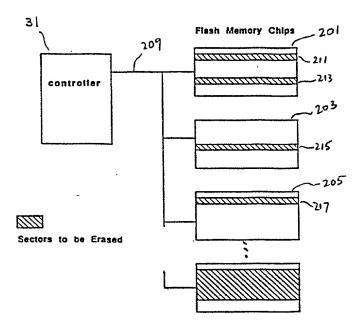
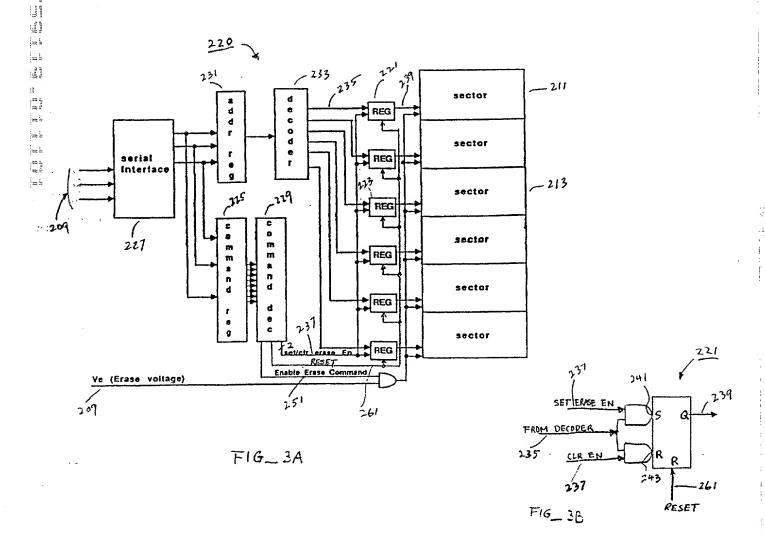
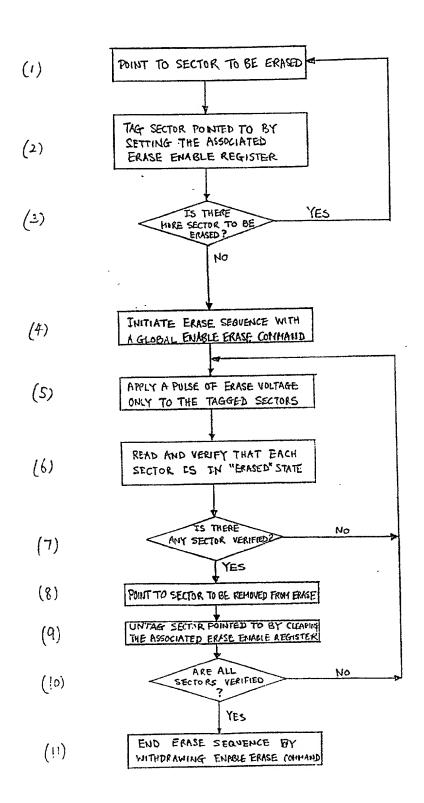
(2 of 6)

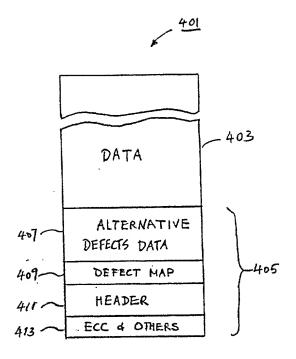


F16\_2





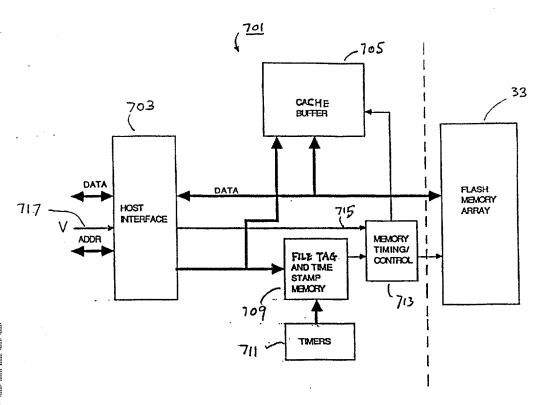
FIG\_4



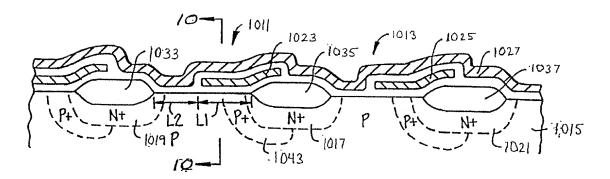
SECTOR PARTITION

F16-5

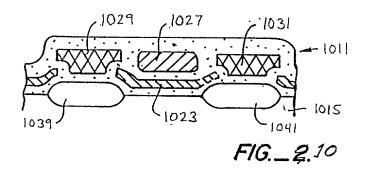
(6 of 6)

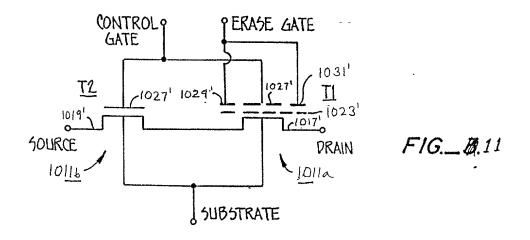


FIG\_8



F1G.\_#,9





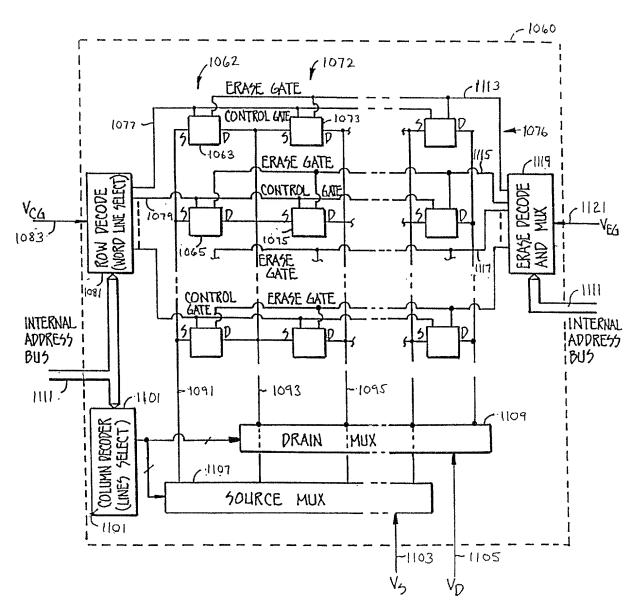


FIG.\_4, 12.

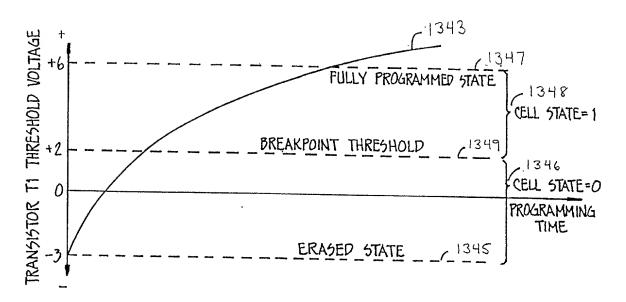


FIG.\_B: 14.

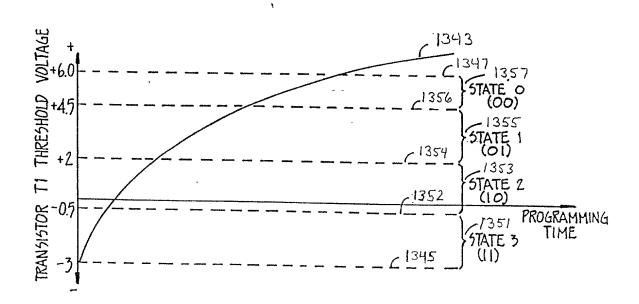


FIG.\_74, 15 A

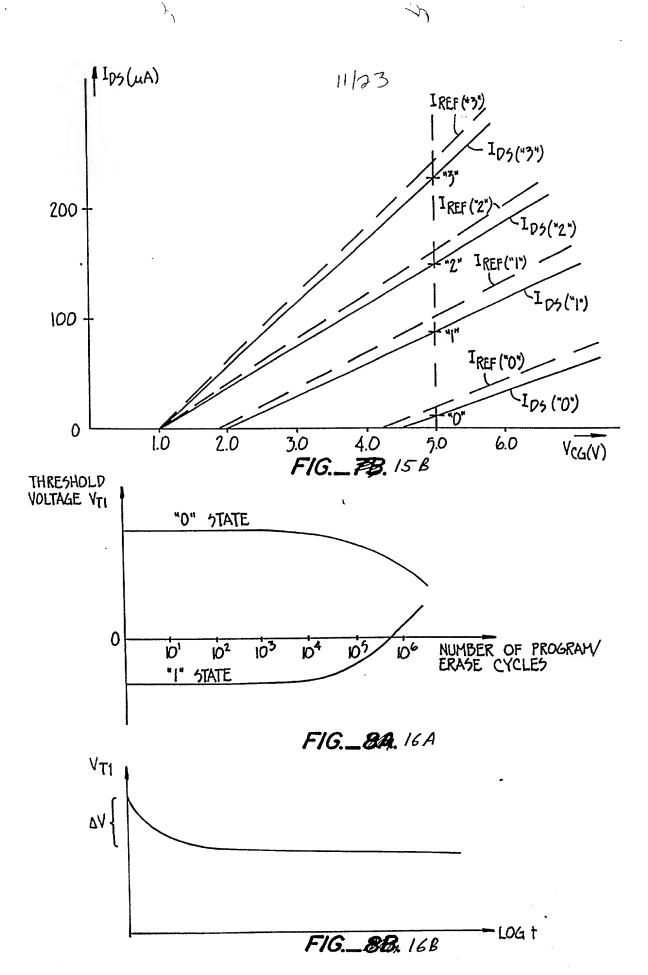


FIG.\_\_81A. 17 A

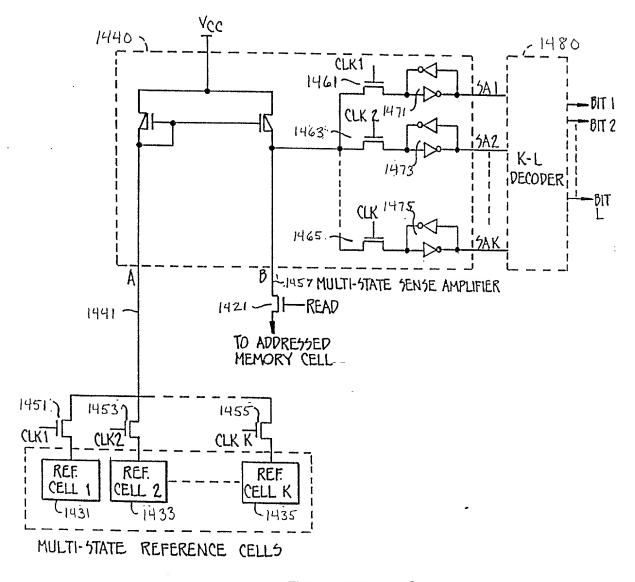
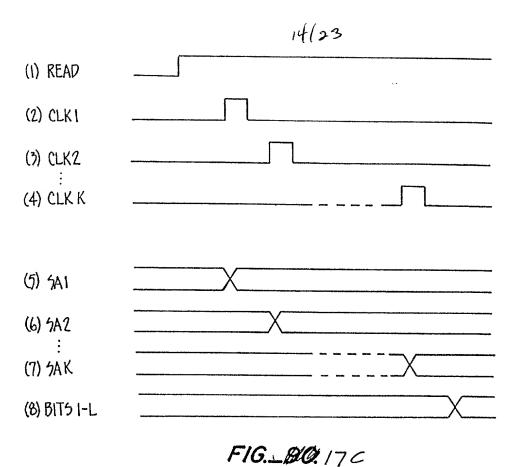
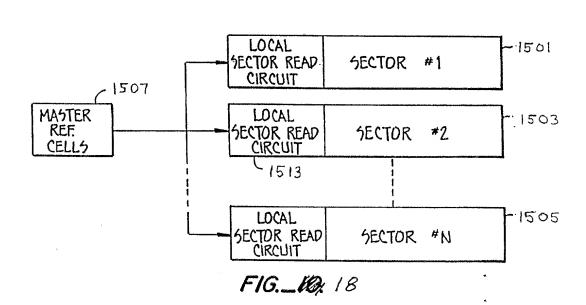
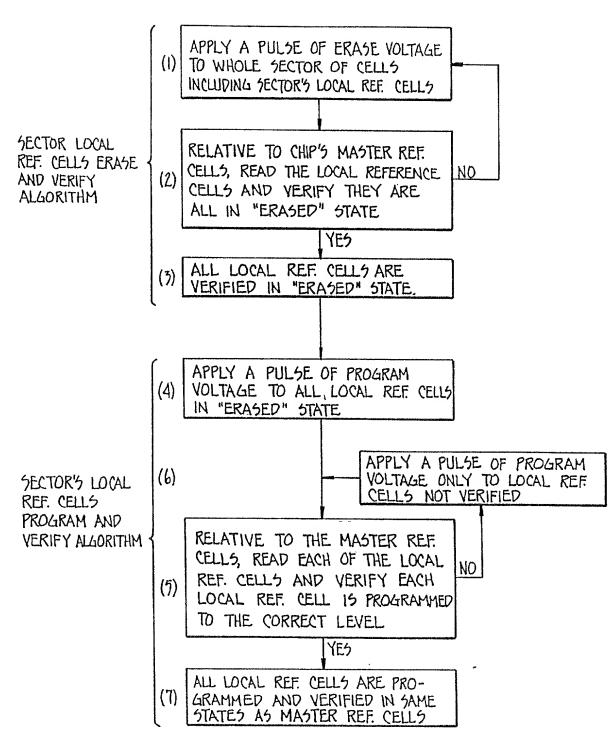


FIG.\_98. 178







na b

22 b

FIG.\_# 19

FIG.\_184. ZIA

Wast Same

as h

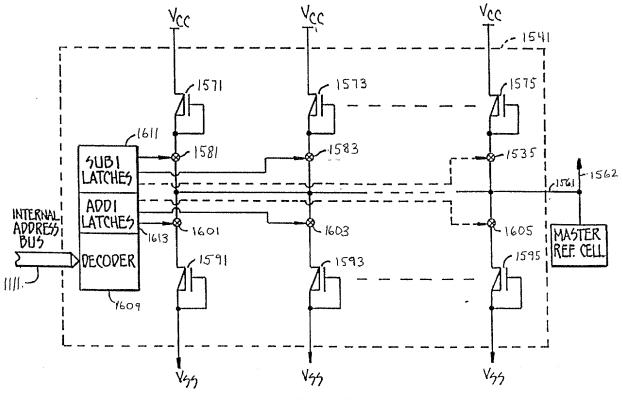
The state of

a b

an b

41

FIG.\_188. 218



F16.186, 21C

LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CEUS

RELATIVE TO THE LOCAL REF. CELLS, READ THE ADDRESSED CELLS

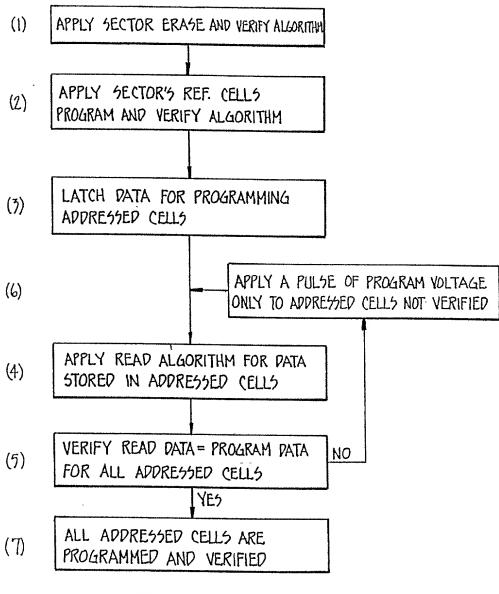
FIG.\_12B, 20B

- (1) LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS
- (2) RELATIVE TO THE LOCAL REFERENCE CELLS READ THE MASTER REF. CELLS
- (3) DETERMINE THE DIFFERENCES, IF ANY AND BIAS. THE MASTER REF CELLS' CURRENT'S SUCH THAT THE SAME READING IS OBTAINED RELATIVE TO THE BIASED MASTER REF. CELLS AS RELATIVE TO THE LOCAL REF. CELLS
- (4) RELATIVE TO THE BIASED MASTER REF. CELLS, READ THE ADDRESSED CELLS

}

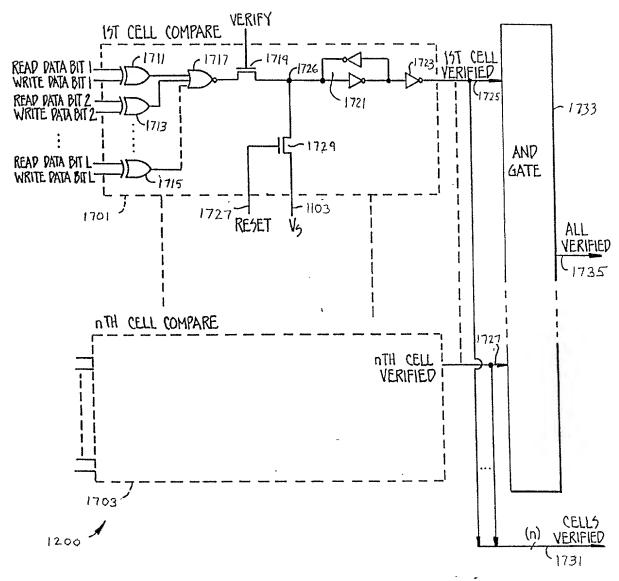
READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG.\_图 22.



PROGRAM ALGORITHM

FIG.\_15. 23



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FIG.\_ 稿. 24

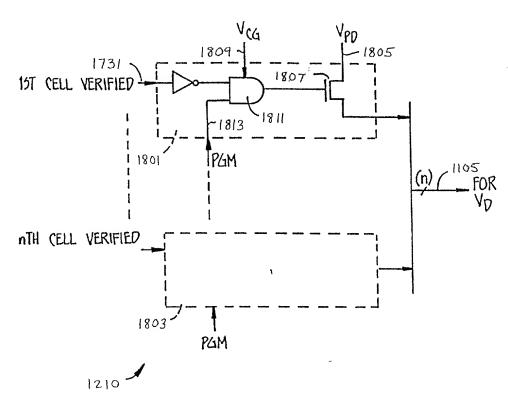


FIG.\_ 1. 25

	SELECTED CONTROL GATE V <sub>CC</sub>	DRAIN V <sub>D</sub>	SOURCE V <sub>s</sub>	ERASE GATE V <sub>EG</sub>
READ	$V_{PG}$	$V_{ ext{\tiny REF}}$	$v_{ss}$	$V_{\rm E}$
PROGRAM	$V_{ m pg}$	$V_{\mathtt{PD}}$	$V_{ss}$	V <sub>E</sub>
PROGRAM VERIFY	$V_{PG}$	$ m V_{REF}$	$V_{ss}$	V <sub>E</sub>
ERASE	$ m V_{PG}$	$ m V_{REF}$	$V_{ss}$	$V_{\rm E}$
ERASE VERIFY	$V_{PG}$	, V <sub>REF</sub>	V <sub>ss</sub>	V <sub>E</sub>

## 100 FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V <sub>PG</sub> .	$v_{cc}$	12v	V <sub>cc</sub> +δV	V <sub>cc</sub>	V <sub>cc</sub> -&V
V <sub>cc</sub>	5v	5 <b>v</b>	5v	5 <b>v</b>	5 <b>v</b>
V <sub>PD</sub>	$v_{ss}$	84	8v	$v_{ss}$	V <sub>ss</sub>
V <sub>E</sub>	V <sub>ss</sub>	Vss	V <sub>ss</sub>	20 <b>v</b>	V <sub>ss</sub>
unselected control gate	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>
unselected bit line	V <sub>REF</sub>	V <sub>REF</sub>	V <sub>REF</sub>	V <sub>REF</sub>	V <sub>REF</sub>

 $V_{ss}=0V$ ,  $V_{REF}=1.5V$ ,  $\delta V=0.5V-1V$